MIT-ADT UNIVERSITY
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# School of Engineering & Sciences

## Department of Electronics & Communication Engineering

# LABORATORY MANUAL

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|---|---|
| **Program:** | **B. Tech. Electronics and Communication Engineering** |
| **Year:** | **First Year** |
| **Course Code:** | **23ECE1203** |
| **Course Name:** | **Electronic Circuits Lab.** |
| **AY:** | **2025-26** **Sem:** **Even** |

## *Experiment No.1*

***Title:-***

***Division:-*** ***Batch:-*** ***Roll no:-***

***Date of Performance:-*** ***Date of Submission:-***

# EXPERIMENT No.1

## Aim: To Study of BJT as a Switch

## Apparatus:

Resistors (10KΩ,4.7KΩ), Transistor (BC547), Regulated DC power supply, Digital Multimeter Breadboard, LED, connecting wires.

## Theory:

Bipolar junction transistors can be used in many applications like amplifiers, switches,oscillator and many others. If the transistor is biased into the active region, it can work as an amplifier whereas if biased in the saturation and cut-off regions, then it is used as a switch.

A switch consists of a BJT transistor that is alternately driven between the saturation and cutoff regions.

When $V_{in}$ is such as to reverse bias the Vbe junction no current flows in the base henceno collector current will flow.

When the BJT is in cutoff, the circuit (ideally) has the following values:

i.e Vin = 0 or less then, VCE = VCC and IC = 0 A In this state BJT acts like an open switch.

When the input equals +Vin, the transistor is driven into saturation and the following conditions occur: i.e Vin = +Vin, Then , VCE 0V and $I_C sat$ = VCC/RC

This state is similar to a closed switch connecting the bottom of $R_C$ to ground.

These conditions can be assured by designing the circuit so that:

1. If Vin is negative or zero, guarantees that the circuit is driven into the cutoff region by the input.
2. $I_B > I_{Csat}/ß$ and $VCE(sat) \leq 0.2V$

An actual BJT switch differs from the ideal switch in several aspects. In practice, even in cutoff there is some leakage current through the transistor. Also, in saturation, there is always some voltage dropped across the transistor's internal resistance. Typically, this will be between 0.2 and 0.4 V in saturation depending on the collector current and size of the device. These variationsfrom the ideal are generally minor with a properly sized device, so we can assume near ideal conditions when analyzing or designing a BJT switch circuit.

## Procedure:

1. Connect the components as shown in circuit diagram.
2. Apply Vcc = 5V from regulated DC power supply.
3. Vary input voltage and measure $V_{BE}$, $V_{CE}$.
4. Check status of LED.

## Circuit Diagram:

## Observation Table:

| Sr. No. | Input Voltage (Vin) | $V_{BE}$(V) | $V_{CE}$(V) | Status of LED |
|---|---|---|---|---|
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## CONCLUSION :

## POST LAB QUESTIONS:

1. What is the role of the base resistor in a transistor switch circuit?
2. Explain the difference between the transistor operating in saturation and cutoff regions. How do these regions relate to the switching function?
3. What happens if the base resistor value is too high or too low? How did this affect the switching performance?
4. What is the purpose of using a transistor as a switch in a circuit?
5. Which type of transistor (NPN or PNP) was used in the lab and why?

*Experiment No.2*

**Title:-**

**Division:-** **Batch:-** **Roll no:-**

**Date of Performance:-** **Date of Submission:-**

# EXPERIMENT No. 2

**Aim:** To plot input & output characteristics of transistor in CE configurations.

**Apparatus:** DC power supply(0-10V), Voltmeter (0-10V), Transistor (BC547), Resistors Currentmeter (0-10mA/0-50μA), Resistor ( (1KΩ, 10KΩ)

## Theory:

Bipolar Junction Transistor (BJT) is a semiconductor device in which the output current conduction in due to majority as well as minority carriers. There are two types of BJT: N-P-N and P-N-P. The arrow is always on the emitter lead and points in the direction of conventional current flow (positive-to-negative).

The device characteristics can be studied in CE, CB and CC configuration by making one of the terminals common for both input and output.

CB/CE/CC Characteristics:

There three characteristics to be studied are:

1. Input characteristics
2. Output characteristics
3. Transfer characteristics

**Input characteristics**:

This is the graph between input current and input voltage at constant output voltage for respective configuration.

**Output characteristics:**

This is the graph between output current and output voltage at constant output voltage for respective configuration.

**Transfer Characteristics:** It shows the relation between input and output current.

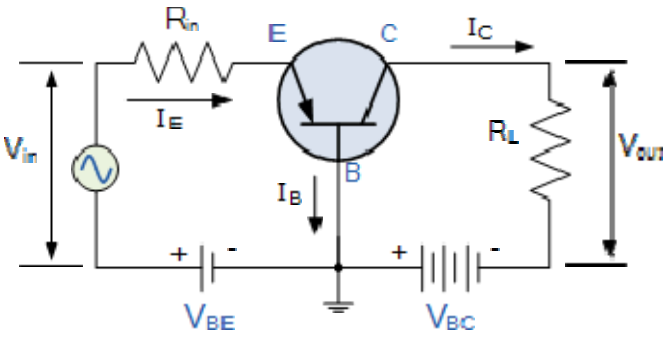
### The Common Base (CB) Configuration

As its name suggests, in the Common Base configuration, the base is common to both the input signal and the output signal. The input signal is applied between the transistors base and the emitter terminals, while the corresponding output signal is taken from between the base and the collector terminals as shown. The base terminal is grounded or can be connected to some fixed reference voltage point.

The input current flowing into the emitter is quite large as its the sum of both the base current and collector current respectively therefore, the collector current output is less than the emitter

current input resulting in a current gain for this type of circuit of "1" (unity) or less, in other words the common base configuration "attenuates" the input signal.

**The Common Base Transistor Circuit**



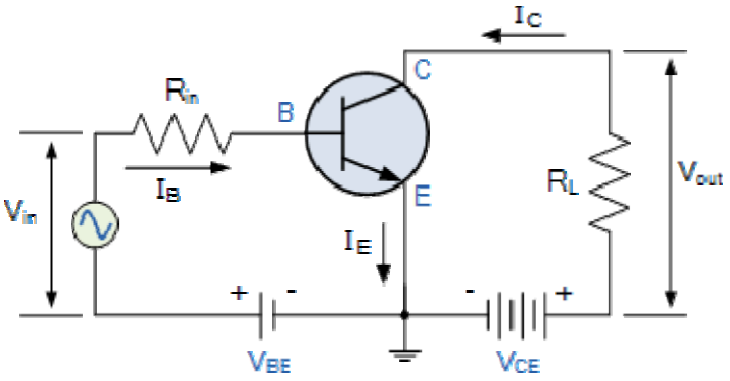

The common base circuit is generally only used in single stage amplifier circuits such as microphone pre-amplifier or radio frequency ( R*f* ) amplifiers due to its very good high frequency response.

**The Common Emitter (CE) Configuration**

In the Common Emitter configuration, the input signal is applied between the base and the emitter, while the output is taken from between the collector and the emitter as shown. This type of configuration is the most commonly used circuit for transistor based amplifiers and which represents the "normal" method of bipolar transistor connection.

The common emitter amplifier configuration produces the highest current and power gain of all the three bipolar transistor configurations. This is mainly because the input impedance is low as it is connected to a forward biased PN-junction, while the output impedance is high as it is taken from a reverse biased PN-junction.

**The Common Emitter Amplifier Circuit**




The current gain of the common emitter transistor configuration is quite large as it is the ratio of Ic/Ib. A transistors current gain is given by Beta (β ).

As the emitter current for a common emitter configuration is defined as Ie = Ic + Ib, the ratio of Ic/Ie is called Alpha, given the Greek symbol of α. Note: that the value of Alpha will always be less than unity.

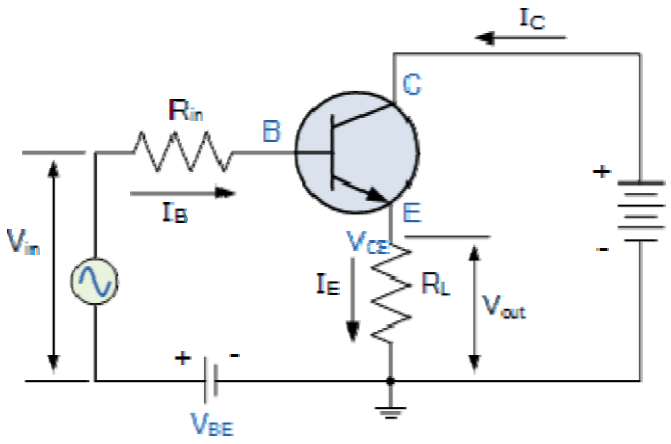
This bipolar transistor configuration has a greater input impedance, current and power gain than that of the common base configuration but its voltage gain is much lower. The common emitter configuration is an inverting amplifier circuit. This means that the resulting output signal has a $180^o$ phase-shift with regards to the input voltage signal.

The Common Collector (CC) Configuration

In the Common Collector configuration, the collector is now common through the supply. The input signal is connected directly to the base, while the output is taken from the emitter load as shown. This type of configuration is commonly known as a Voltage Follower or Emitter Follower circuit.

The common collector, or emitter follower configuration is very useful for impedance matching applications because of the very high input impedance, in the region of hundreds of thousands of Ohms while having a relatively low output impedance.

**The Common Collector Transistor Circuit**




In the common collector configuration the load resistance is situated in series with the emitter so its current is equal to that of the emitter current.

The current gain of the circuit is given as:

This type of bipolar transistor configuration is a non-inverting circuit in that the signal voltages of Vin and Vout are "in-phase". It has a voltage gain that is always less than "1" (unity).

The load resistance of the common collector transistor receives both the base and collector currents giving a large current gain (as with the common emitter configuration) therefore, providing good current amplification with very little voltage gain.

After cut-in voltage the base current increases rapidly with small increase in base emitter voltage. These indicate the dynamic input resistance is small in CE configuration.

| Type | $V_{CE(Sat)}$ | $V_{BESAT}$ | $V_{BE(active)}$ | $V_{BE(cutin)}$ | $V_{BE(cutoff)}$ |
|---|---|---|---|---|---|
| Si | 0.2 | 0.8 | 0.7 | 0.5 | 0.0 |
| Ge | 0.1 | 0.3 | 0.2 | 0.1 | -0.1 |

**CIRCUIT DIAGRAM:**

**PROCEDURE:**

Procedure for Input characteristics of CE configuration: -

1. Make the connection as per the diagram.
2. Keep the collector to emitter voltage constant at 0V.
3. Vary the $I_B$ from 0 to 30μA as per the steps mentioned in the observation table and Note down corresponding base to emitter voltage ($V_{BE}$)
4. Repeat the above procedure for $V_{CE}$= 4V (precaution must be taken that in any case $I_B$ should not exceed 60μA)
5. Plot the input characteristics ($V_{BE}$ Vs $I_B$ for constant values of $V_{CE}$ ) on graph paper.

Procedure for Output characteristics of CE configuration: -

1. Make the connection as per the diagram.
2. Keep the base current constant at 5μA.
3. Vary the voltage $V_{CE}$ from 0 to 10V as per the steps mentioned in the observation table and Note down the corresponding collector current ($I_C$)
4. Repeat the above procedure for $I_B$= 10μA, 15μA, 20μA (precaution must be taken that in any case $I_B$ should not exceed 60μA)
5. Plot the output characteristics ($V_{CE}$ Vs $I_C$ for constant values of $I_B$) on graph paper.

**OBSERVATION TABLE:**

**INPUT CHARACTERISTICS**

| Sr.No. | Vin (V) | $V_{BE}$ (V) | $I_B$ (μA) | |
|---|---|---|---|---|
| | | | $V_{CE}$ = 0V | $V_{CE}$ = 5V |
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## OUTPUT CHARACTERISTICS

| Sr.No. | $V_{CE}$ (V) | $I_C$ (mA) | | | |
|---|---|---|---|---|---|
| | | $I_B$ =5μA | $I_B$ =10μA | $I_B$ =15μA | $I_B$ = 20μA |
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**GRAPHS** : 1. INPUT CHARACTERISTICS

2. OUTPUT CHARACTERISTICS

## CONCLUSION :

## POST LAB QUESTIONS:

:

1. BJT is bipolar device justify.
2. BJT is current controlled device justify.
3. Give the equation of collector current in different configuration?
4. Name the three characteristics of BJT
5. Which are the three region of operation of BJT? Give region wise application.

## *Experiment No.3*

***Title:-***

***Division:-*** ***Batch:-*** ***Roll No:-***

***Date of Performance:-*** ***Date of Submission:-***

# EXPERIMENT No. 3

**Aim:** Study biasing circuits of BJT

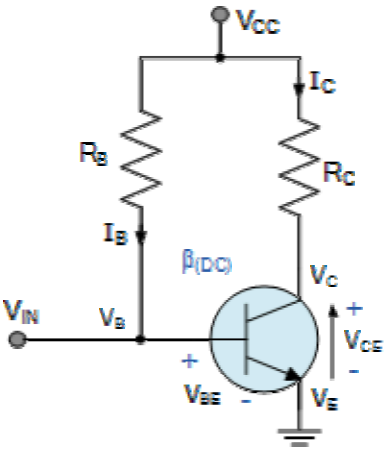
**Apparatus:** Resistors (470KΩ,1KΩ,10KΩ,4.7KΩ), Transistor (BC547), Regulated DC power supply, Digital Multimeter, Breadboard, connecting wires.

**Theory:**
The base, collector currents and collector voltage decides the operation of a transistor. To operate the transistor in required region it must be biased properly.
Some of the common transistor biasing circuits are:

1. Fixed bias
2. Collector to base bias
3. Voltage divider or self bias

**Fixed Bias:**

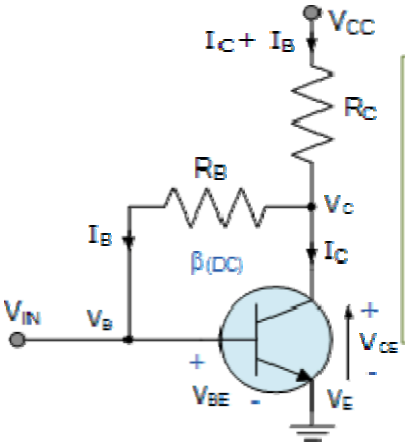
The transistors base current, $I_B$ remains constant for given values of Vcc, and hence the transistors operating point remains fixed. Resistor Rc and Rb network is used to establish the




$V_C = V_{CC} - (I_C R_C)$
$V_{CE} = V_C - V_E$
$V_E = 0v$
$V_B = V_{BE}$
$I_B = \frac{V_{CC} - V_{BE}}{R_B}$
$I_C = \beta_{(DC)} I_B$
$I_E = (I_C + I_B) \cong I_C$

operating region of the transistor.
The current via resistor Rb biases the emitter junction of the transistor is forward biased.
Then the value of $R_B$ is simply: $(V_{CC} – V_{BE})/I_B$ where $I_B$ is defined as $I_C/\beta$.
In this biasing method the biasing voltages and currents do not remain stable during transistor operation and can vary. Also the temperature of the transistor can also affect the operating point of the transistor.

**Collector to base bias:**



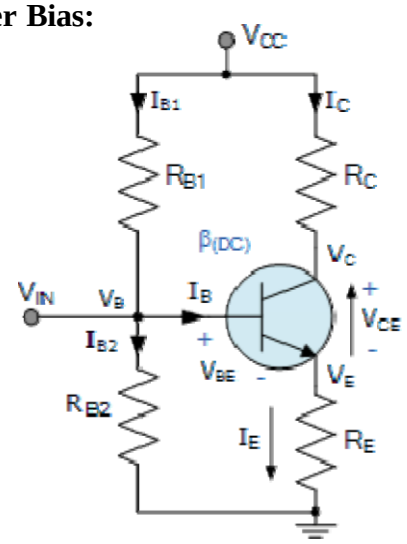

$V_C = V_{CC} - R_C(I_C + I_B)$
$V_E = 0v$
$V_B = V_{BE}$
$I_B = \frac{V_C - V_B}{R_B}$
$I_C = \beta_{(DC)} I_B$
$I_E = (I_C + I_B) \cong I_C$

The collector to base feedback resistor configuration ensures that the transistor is always biased in the active region. The base resistor, $R_B$ is connected to the transistors collector. If the collector current increases, the collector voltage drops, reducing the base voltage and thereby reducing the collector current to keep the transistors Q-point fixed. This method of collector feedback biasing through resistor Rb produces negative feedback as there is feedback from the output to the input.

If the load current increases there will be a larger voltage drop across Rc, and a correspondingly the collector voltage will reduce. Which will cause a corresponding drop in the base current $I_B$, which in turn, will compensate the change and $I_C$ by reducing it.

The opposite reaction will also occur when transistors collector current becomes less. Then this method of biasing is called self-biasing with the transistors stability using this type of feedback bias network being generally good for most amplifier designs.

**Voltage Divider Bias:**




$V_C = V_{CC} - R_C I_C = (V_E + V_{CE})$
$V_E = I_E R_E = V_B - V_{BE}$
$V_{CE} = V_C - V_E = V_{CC} - (I_C R_C + I_E R_E)$
$V_B = V_{BE} + V_E = V_{RB2} = \left(\frac{R_{B2}}{R_{B1} + R_{B2}}\right) V_{CC}$
$I_{B2} = \frac{V_B}{R_{B2}}$
$I_{B1} = I_B + I_{B2} = \frac{V_{CC} - V_B}{R_{B1}}$
$R_B = \frac{R_{B1} \times R_{B2}}{R_{B1} + R_{B2}}$
$I_B = \frac{V_B - V_{BE}}{R_B + (1+\beta) R_E}$
$I_C = \beta_{(DC)} I_B$
$I_E = I_C + I_B = \frac{V_E}{R_E}$

The common emitter transistor is biased using a voltage divider network to increase stability. The name of this biasing configuration comes from the fact that the two resistors RB1 and RB2 form a voltage or potential divider network across the supply with their center point junction connected the transistors base terminal as shown.

This voltage divider biasing configuration is the most widely used transistor biasing method, as the emitter diode of the transistor is forward biased by the voltage dropped across resistor RB2. Also, voltage divider network biasing makes the transistor circuit independent of changes in beta as the voltages at the transistors base, emitter, and collector are dependent on external circuit values.

To calculate the voltage developed across resistor RB2 and therefore the voltage applied to the base terminal we simply use the voltage divider formula for resistors in series.

Generally, the voltage drop across resistor RB2 is much less than for resistor RB1. Then clearly the transistors base voltage VB with respect to ground, will be equal to the voltage across RB2.

The current flowing through resistor RB2 is generally set at 10 times the value of the required base current IB so that it has no effect on the voltage divider current or changes in Beta.

The goal of Transistor Biasing is to establish a known Q-point in order for the transistor to work efficiently and produce an undistorted output signal. Correct biasing of the transistor also establishes its initial AC operating region with practical biasing circuits using either a two or four-resistor bias network.

In bipolar transistor circuits, the Q-point is represented by ( $V_C$, $I_C$ ) for the NPN transistors or ( $V_{EC}$, $I_C$ ) for PNP transistors. The stability of the base bias network and therefore the Q-point is generally assessed by considering the collector current as a function of both Beta (β) and temperature.
Here we have looked briefly at five different configurations for "biasing a transistor" using resistive networks. But we can also bias a transistor using either silicon diodes, zener diodes or active networks all connected to the base terminal of the transistor or by biasing the transistor from a dual power supply.

**Procedure:**

1. Connect the components as shown in circuit diagram.
2. Apply Vcc from regulated DC power supply.
3. Measure $V_{CEQ}$, $I_{CQ}$ on multimeter.
4. Compare theoretical result with practical value.

**Circuit Diagram:**

**Observation Table:**

| Biasing Circuit | Calculated Value | | Measured Value | |
|---|---|---|---|---|
| | $V_{CEQ}$ | $I_{CQ}$ | $V_{CEQ}$ | $I_{CQ}$ |
| Fixed Bias | | | | |
| Collector to base bias | | | | |
| Voltage Divider Bias | | | | |

**Calculations:**

## CONCLUSION :

## POST LAB QUESTIONS:

1. Why is biasing necessary in BJT circuits? What would happen if a BJT is not properly biased?
2. Which biasing circuit (fixed bias, collector-to-base bias, voltage divider bias, etc.) offers the best thermal stability and why?
3. Explain how the DC load line and the Q-point (quiescent point) relate to the proper operation of a BJT.
4. Why is the voltage divider bias configuration commonly preferred over other types of biasing circuits?
5. Write formula for stability factor for fixed bias, collector-to-base bias, voltage divider bias.

## *Experiment No.4*

***Title:-***

***Division:-*** ***Batch:-*** ***Roll. No:-***

***Date of Performance:-*** ***Date of Submission:-***

# EXPERIMENT No. 4

**Aim:** To calculate Gain of CB / CC amplifier.

**Apparatus:** POWER SUPPLY(0-10V), CRO(0-20MHz), SIGNAL GENERATOR(0-1MHz)

**THEORY:**

BJT can be used as two port device by making one of the terminal common for input and output. According to this we can have following possible configurations CB, CE ans CC.

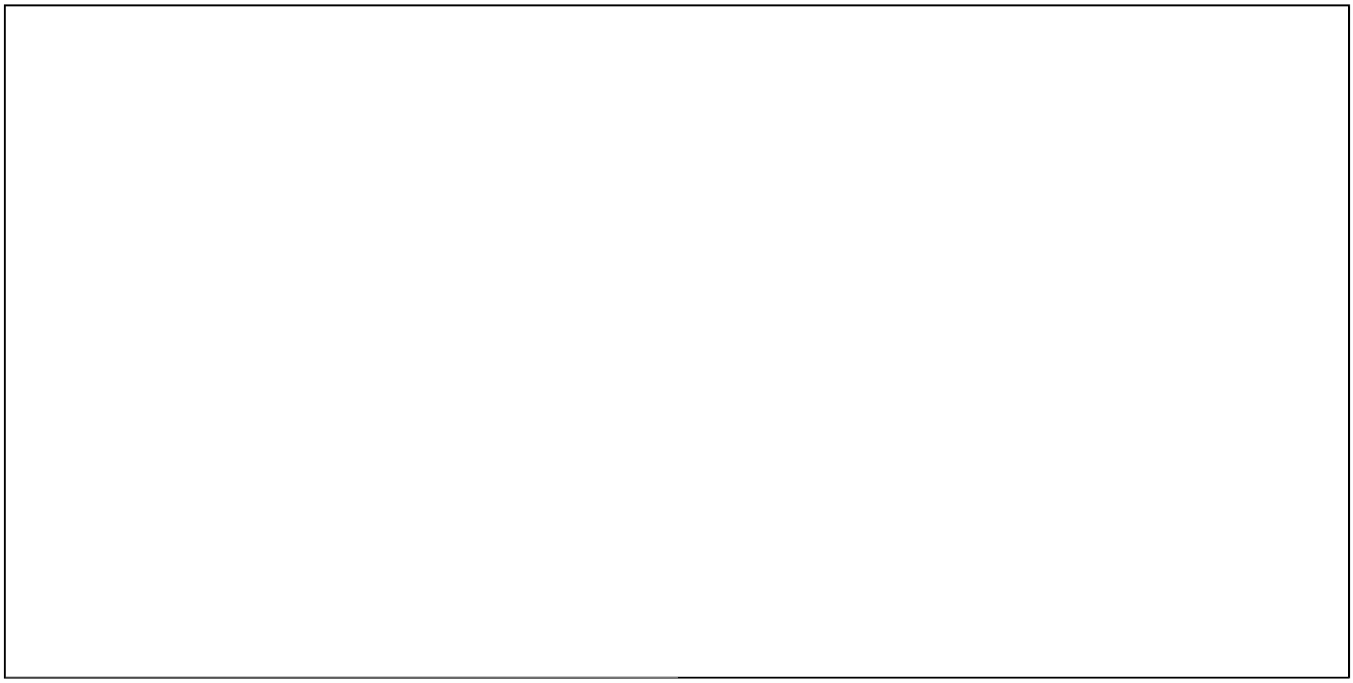
1. **CB amplifier:**
   In this configuration input appears between emitter and base where as output appears between collector and base. The base terminal is common for input and output and is at minimum potential in the circuit. In this circuit current gain is closed to unity, moderate value of voltage gain, very low input resistance and very high output resistance.
   Application: This circuit find application in constant current source circuit.

2. **CE amplifier:**
   In this configuration input appears between base and emitter whereas output appears between collector and emitter. The emitter terminal is common for input and output and is at minimum potential in the circuit. This configuration is widely used because the device offers good values of voltage and current gain and moderate dynamic input resistance and high dynamic output resistance. This configuration is also preferred in electronic switch application, because the switch operation is possible at low value of input voltage and current.
   Application: This configuration is used as an amplifier and as a switch.

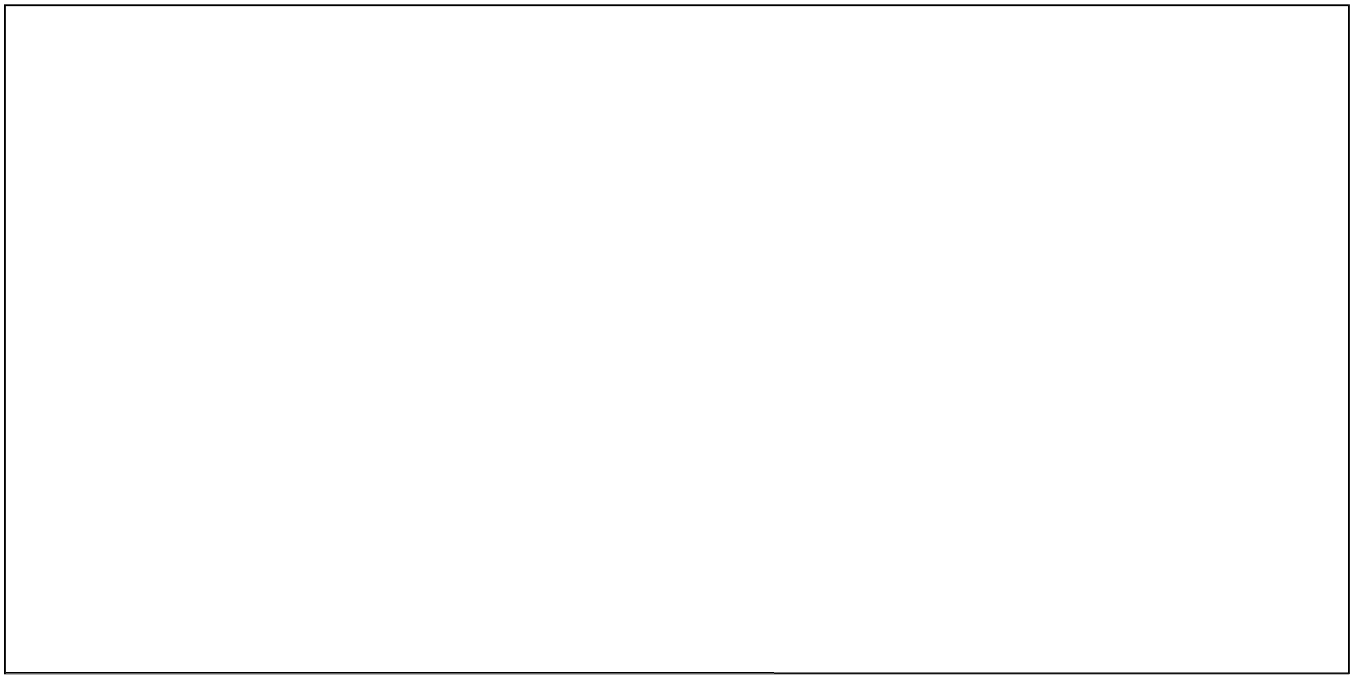
3. **CC amplifier:**
   In this configuration input appears between base and collector whereas output appears between emitter and collector. The collector terminal is common for input and output and is at minimum potential in the circuit. In this configuration, junction at the input (collector -base) is reverse biased condition, and the junction at the output (emitter- base) is in the forward biased. Hence this configuration has very high input resistance and low output resistance. Also this circuit offers very high current gain and voltage gain close to unity.
   Application: This configuration is preferred in buffer circuit. The cascading of two CC stages forms a Darlington emitter follower, which is used as a driver circuit.

**CIRCUIT DIAGRAM:**

**CB Amplifier:**



**CC amplifier**



**PROCEDURE**

## A. Common Base (CB) Amplifier Simulation in Multisim

1. Open Multisim & Create a New Circuit
   - Launch Multisim and open a new project.
   - Select components from the component library.

2. Select and Place Components
   - NPN BJT transistor (e.g., BC547 or 2N2222), Resistors, Capacitors, Power Supply, AC Signal Source, Ground connection

3. Design the CB Amplifier Circuit
   - Connect the input signal to the emitter terminal.
   - Connect the collector to a resistor Rc and then to Vcc.
   - The base is grounded through a biasing network.
   - Use coupling capacitors to block DC and pass AC signals.

4. Set Component Values
   - Choose appropriate values, e.g.:
   - RB=470kΩ, RC=4.7kΩ, RE=1kΩ
   - C1=10μF, C2=10μF,
   - VCC=12V

5. Run the Simulation

   Apply a small AC signal (e.g., 10mV, 1kHz) to the emitter. Use an oscilloscope to measure input and output voltages.

6. Calculate Voltage Gain (AV)
   - Measure the output voltage (Vout) at the collector.
   - Measure the input voltage (Vin) at the emitter.
   - Voltage Gain Formula: AV= Vout / Vin
   - Since CB amplifiers have high voltage gain, expect $AV \gg 1$

## B. Common Collector (CC) Amplifier Simulation in Multisim

1. Open Multisim & Create a New Circuit
   - Follow the same steps as the CB amplifier setup.

2. Select and Place Components
   - Use an NPN BJT transistor (e.g., BC547 or 2N2222).
   - Resistors: RB, RC, RE.
   - Capacitors: Coupling capacitors.

- AC Signal Source and DC Power Supply.

3. Design the CC Amplifier Circuit
   - Connect the input signal to the base through a capacitor.
   - The collector is directly connected to Vcc.
   - The output is taken from the emitter.
   - Place an emitter resistor RE to improve stability.

4. Set Component Values
   - Typical values:
     - RB=470kΩR, RC=1kΩ, RE=4.7kΩ, C1=10μF, C2=10μF,
     - VCC=12V

5. Run the Simulation
   - Apply a small AC signal (e.g., 10mV, 1kHz) at the base.
   - Use an oscilloscope to measure input and output voltages.

6. Calculate Voltage Gain (AV)
   - Measure the input voltage (Vin) at the base.
   - Measure the output voltage (Vout) at the emitter.
   - Voltage Gain Formula: AV= Vout / Vin
   - Since CC amplifiers have gain ≈ 1 (slightly less), expect AV ≈ 0.9−1

**OBSERVATION TABLE:**

**COMMON BASE AMPLIFIER**

| $V_{in}$ | $V_{Out}$ | $Av = \frac{Vout}{Vin}$ |
|---|---|---|
| | | |

**COMMON COLLECTOR AMPLIFIER**

| $V_{in}$ | $V_{Out}$ | $Av = \frac{Vout}{Vin}$ |
|---|---|---|
| | | |

**FORMULA**

$$Av = \frac{Vout}{Vin}$$

Where, Av= Voltage Gain Vin = Input Voltage Vout = Output Voltage

**CALCULATION:**

| 1. CB amplifier | 2. CC amplifier |
|---|---|
| | |

**RESULT**

| Parameter | CB amplifier | CC amplifier |
|---|---|---|
| $A_V$ | | |

## CONCLUSION :

## POST LAB QUESTIONS:

1. Why does a CB amplifier have a high voltage gain, while a CC amplifier has a gain close to 1?
2. What is the phase relationship between the input and output signals for CB amplifier and CC amplifier?
3. Where is a CC amplifier commonly used?
4. What is the function of coupling capacitors in these amplifiers?
5. How do the values of $R_C$ and $R_E$ affect the gain of the CB and CC amplifiers?

***Experiment No.5***

***Title:-***

***Division:-*** ***Batch:-*** ***Roll no:-***

***Date of performance:-*** ***Date of Submission:-***

# EXPERIMENT No.5

**AIM:** To Plot I-V characteristics of JFET.

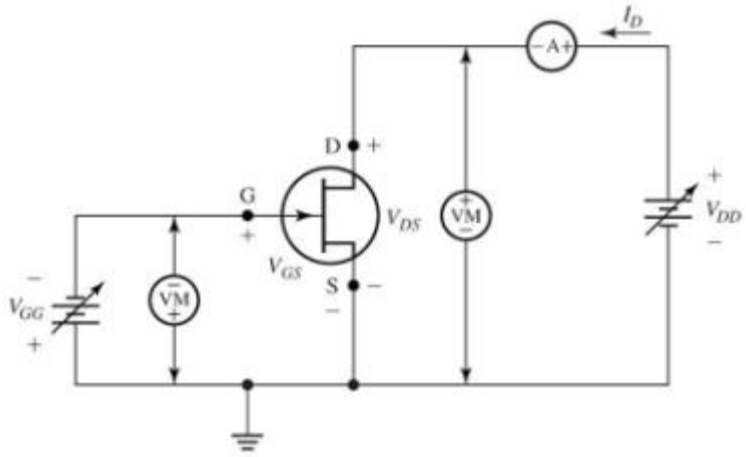
**APPARATUS:** Power Supply, BFW 10, resistors

## THEORY:

The phenomenon of modulating (changing) conduction of a semiconductor material by anelectric field applied perpendicular to the surface of a semiconductor is known as **field effect**. There are two general classes of FETs a) Junction FET and b) Metal Oxide Semiconductor FET (MOSFET). A JFET in conjunction with other circuit elements is capable of providing voltage gain. A JFET can be n-channel or p-channel type. Figure 1 shows the construction of n-channel JFET. Ohmic contacts are made to two sides of n-type silicon bar. There are three terminals for this symmetrical JFET. They are a) Source (S) b) Gate (G) and c) Drain (D). The conventional current entering these terminals are designated as $I_S$, $I_G$ and $I_D$ respectively. The terminal voltage between G and S terminals is $V_{GS}$, that between D and S is $V_{DS}$. Normally gate-source junctionof JFET is reverse biased. Hence there is no $I_G$ (at least in theory) for JFET.

Gate region of JFET is heavily doped (p+). Electrons, which are majority carriers for n- channel device, are assumed to originate at S terminal. The width of "channel" existing between S and D depends upon $V_{GS}$. The channel is (maximum) open for $V_{GS} = 0$. Channel width reduceswhen we apply more negative $V_{GS}$. This is because of penetration of depletion region into channel. When channel width reduces, the drain current tends to reduce.

## CIRCUIT DIAGRAM:



If we apply small $V_{DS}$, the drain current flows. Since channel is maximum open for $V_{GS}$ =0, drain current is maximum. This is denoted by $I_{DSS}$. For small values of $V_{DS}$, the relation between $I_D$ and $V_{DS}$ is linear, for a given $V_{GS}$. This region of drain characteristics is known as **Ohmic region**. If we increase $V_{GS}$ (make it more negative), the channel constricts, until finally itreaches a condition called pinch-off. For this condition, the drain current almost levels-off and does not increase with $V_{DS}$, as in ohmic region. The value of $V_{DS}$ for which $I_D$ reaches maximum value, under the condition of $V_{GS}$ = 0, is known as **Pinch-off Voltage** ($V_p$).

For a given $V_{GS}$, the drain current levels-off after pinch-off voltage and does not change with $V_{DS}$. The region to the right of pinch-off voltage is known as **Triode or Saturation region**. Since the electric fields due to $V_{DS}$ and $V_{GS}$ interact with each other, pinch-off occurs at lesser voltages for more negative $V_{GS}$. The graph of $I_D$ versus $V_{DS}$, for a given vale of $V_{GS}$ is drain characteristic of JFET.

If we plot the relation $I_D$ versus $V_{GS}$, we get what is known as transfer characteristic of JFET. This transfer characteristic exhibit a square law relation governed by Shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad V_P = V_{GS(OFF)}$$

The slope of transfer characteristic varies at different points on it. The slope is maximumat $V_{GS}$ = 0 and it is defined to be a parameter $g_{mo}$. Thus

$$g_{mo} = -\frac{2IDSS}{VP}$$

For a given JFET, $g_{mo}$ is the value of maximum transconductance. In general, thetransconductance $g_m$ is-

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

When $V_{GS}$ reaches a value where $I_D$ becomes zero, it is designated as $V_{GS(OFF)}$. For agiven JFET, $V_{GS(OFF)}$ and $V_p$ are equal in magnitude and opposite in sign.

**A C Drain resistance (rd):**

It is also called dynamic drain resistance and is the a.c.resistance between the drain and source terminal, when the JFET is operating in the pinch off or saturation region.

It is given by the ratio of small change in drain to source voltage ΔVds to the corresponding change

in drain current ΔId for a constant gate to source voltage Vgs. Mathematically it is expressed as rd=ΔVds/ ΔId where Vgs is held constant.

**TRANCE CONDUCTANCE (gm):**

It is also called forward transconductance . It is given by the ratio of small change in drain current (ΔId) to the corresponding change in gate to source voltage (ΔVds)
Mathematically the transconductance can be written as gm=ΔId/ΔVds

**AMPLIFICATION FACTOR (μ)**

It is given by the ratio of small change in drain to source voltage (ΔVds) to the corresponding change in gate to source voltage (ΔVgs)for a constant drain current (Id).
Thus μ=ΔVds/ΔVgs when Id held constant
The amplification factor μ may be expressed as a product of transconductance (gm)and ac drain resistance (rd)
μ=ΔVds/ΔVgs=gm rd

Thus IDSS ,Vp, gm , gmo and VGS(OFF) are important performance parameters studied in this experiment for given JFET.

**CIRCUIT DIAGRAM :**

**Drain characteristics**

**PROCEDURE:**

1. Make the connection as per the diagram.
2. Keep the gate source voltage constant 0V.
3. Vary the $V_{DS}$ from 0 to 10V as per the steps mention in the observation table.
4. Note down the reading of $I_D$.
5. Repeat the above procedure for different $V_{GS}$= -1v, -1.5v. **(precaution must betaken that in any case $V_{GS}$ should not exceed +0.5 volts)**
6. Plot the drain characteristics ($V_{DS}$ Vs $I_D$ for constant values of $V_{GS}$ ) on graph paper and find out $r_d$ as well as $V_P$ from it.

**Transfer Characteristic**s

**PROCEDURE:**

1. Make the connection as per the diagram.
2. Keep the drain to source voltage constant 5V.
3. Vary the $V_{GS}$ from 0v to $V_{GS(off)}$ in the steps as mention in the observation table, note down the corresponding value of $I_D$.

**OBSERVATION TABLE :**

**DRAIN CHARACTERISTICS**

| Sr.No. | $V_{DS}$ (V) | ID(mA) | | |
|---|---|---|---|---|
| | | $V_{GS}$= | $V_{GS}$= | $V_{GS}$= |
| | | | | |
| | | | | |
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| | | | | |
| | | | | |
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## TRANSFER CHARACTERISTICS

| Sr.No. | $V_{GS}$ (V) | $I_D$ (mA) |
|---|---|---|
| | | $V_{DS}$=5V |
| | | |
| | | |
| | | |
| | | |
| | | |
| | | |
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| | | |

**CALCULATION:**

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad V_P = V_{GS(OFF)}$$

**GRAPHS:** 1. DRAIN CHARACTERISTICS

2. TRANSFER CHARACTERISTICS

**RESULT:**

| Parameter | PRACTICALLY | AS PER DATASHEET |
|---|---|---|
| $r_d$ | | |
| $V_P$ | | |
| $g_m$ | | |
| gmo | | |
| $I_{DSS}$ | | |
| $V_{GS(OFF)}$ | | |
| μ | | |

## CONCLUSION :

## POST LAB QUESTIONS:

1. JFET is voltage-controlled device, justify?
2. JFET is unipolar device justify?
3. Under what condition $I_{DSS}$ and $g_{mo}$ are defined?
4. Some JFET have 4 terminals. What are the $4^{th}$ terminal called as? What is its purpose?
5. Can you derive transfer characteristics of JFET from Drain (output) characteristics? Explain?

## *Experiment No.6*

***Title:***

***Division:*** ***Batch:*** ***Roll No:-***

***Date of Performance:-*** ***Date of Submission:-***

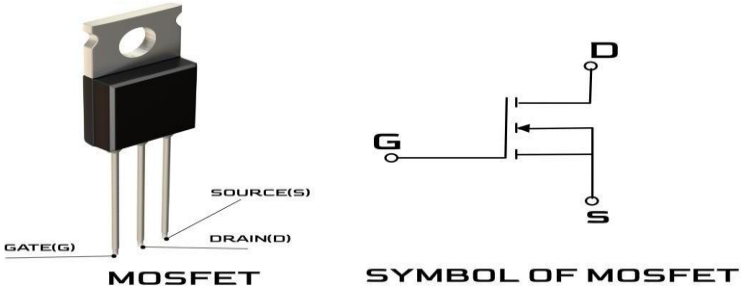
## EXPERIMENT No. 6

**Aim:** To study MOSFET CS Amplifier

**Apparatus: NI Multisim Software** (Any version that supports simulation of analog circuits)

**Theory:**

Metal Oxide Semiconductor Field Effect Transistor, or MOSFET for short, is an excellent choice for small signal linear amplifiers as their input impedance is extremely high making them easy to bias. But for a MOSFET to produce linear amplification, it has to operate in its saturation region, unlike the Bipolar Junction Transistor. But just like the BJT, it too needs to be biased around a centrally fixed Q- point.



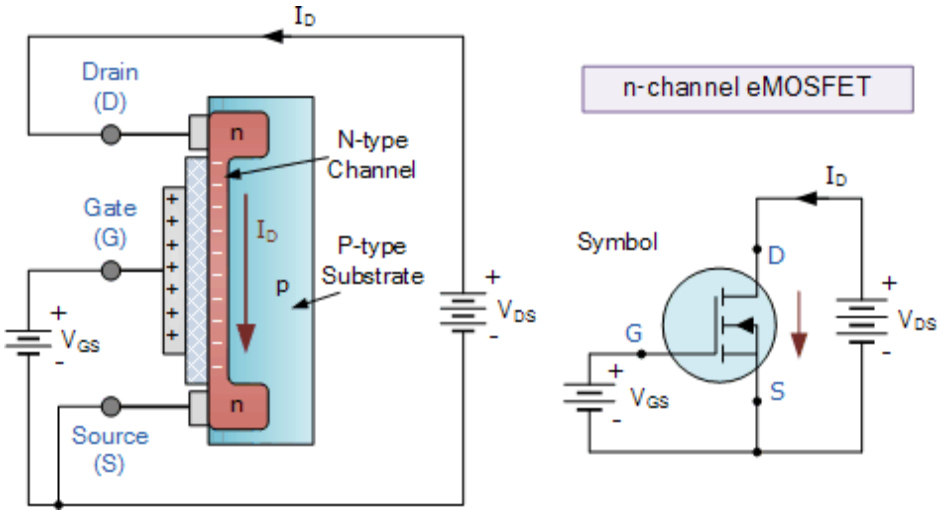

**A Typical MOSFET Transistor**

MOSFETS pass electric current through a conductive region or path called “the channel”. We can make this conductive channel wider or smaller by applying a suitable gate potential.

An electric field induced around the gate terminal by the application of this gate voltage affects the electrical characteristics of the channel, thus the name field-effect transistor.

In other words, we can control how the MOSFET operates by creating or “enhancing” its conductive channel between the source and drain regions producing a type of MOSFET commonly called an n- channel Enhancement-mode MOSFET. This simply means that unless we bias them positively on the gate (negatively for the p-channel), no channel current will flow. There are large variations in the characteristics of different types of MOSFETs, and hence the biasing of a MOSFET must be done individually. As with the bipolar transistor common emitter configuration, the common source MOSFET amplifier needs to be biased at a suitable quiescent value. But first let’s remind ourselves of the MOSFET basic characteristics and configuration.

**Enhancement MOSFET Amplifier**



Enhancement MOSFET, or eMOSFET, can be classed as normally-off (non-conducting) devices, that is they only conduct when a suitable gate-to-source positive voltage is applied, unlike Depletion type MOSFETs which are normally-on devices conducting when the gate voltage is zero. However, due to the construction and physics of an enhancement type MOSFET, there is a minimum gate-to-source voltage, called the threshold voltage VTH that must be applied to the gate before it starts to conduct allowing drain current to flow. An enhancement MOSFET does not conduct when the gate-source voltage, VGS is less than the threshold voltage, VTH but as the gates forward bias increases, the drain current, ID (also known as drain-source current IDS) will also increase, similar to a bipolar transistor, making the eMOSFET ideal for use in MOSFET amplifier circuits.

The characteristics of the MOS conductive channel can be thought of as a variable resistor that is controlled by the gate. The amount of drain current that flows through this n-channel therefore depends on the gate-source voltage and one of the many measurements we can take using a MOSFET is to plot a transfer characteristics graph to show the i-v relationship between the drain current and the gate voltage as shown.
N-channel eMOSFET I-V Characteristics

With a fixed VDS drain-source voltage connected across the eMOSFET we can plot the values of drain current, ID with varying values of VGS to obtain a graph of the MOSFETs forward DC characteristics. These characteristics give the transconductance, gm of the transistor.
This transconductance relates the output current to the input voltage representing the gain of the transistor. The slope of the transconductance curve at any point along it is therefore given as: gm = ID/VGS for a constant value of VDS. gm is called the transistors static or DC transconductance which is short for “transfer conductance” and is given the unit of Siemens (S), as its amps per volt. Voltage gain of a MOSFET amplifier is directly proportional to the transconductance and to the value of the drain resistor.

At VGS = 0, no current flows through the MOS transistors channel because the field effect around the gate is insufficient to create or “open” the n-type channel.
Then the transistor is in its cut-off region acting as an open switch. In other words, with zero gate voltage applied the n-channel eMOSFET is said to be normally-off and this “OFF” condition is represented by the broken channel line in the eMOSFET symbol (unlike the depletion types that have a continuous channel line).

As we now gradually increase the positive gate-source voltage VGS , the field effect begins to enhance the channel regions conductivity and there becomes a point where the channel starts to to conduct. This point is known as the threshold voltage VTH. As we increase VGS more positive, the conductive channel becomes wider (less resistance) with the amount of drain current, ID increases as a result. Remember that the gate never conducts any current as its electrical isolated from the channel giving a MOSFET amplifier an extremely high input impedance.
Therefore the n-channel enhancement MOSFET will be in its cut-off mode when the gate-source voltage, VGS is less than its threshold voltage level, VTH and its channel conducts or saturates when VGS is above this threshold level. When the eMOS transistor is operating in the saturation region the drain current, ID is given by:

eMOSFET Drain Current

$$I_D = k(V_{GS} - V_{TH})^2$$

Note that the values of k (conduction parameter) and VTH (threshold voltage) vary from one eMOSFET to the next and cannot be physically changed. This is because they are specific specification relating to the material and device geometry which are in-built during the fabrication of the transistor.

The static transfer characteristics curve on the right is generally parabolic (square law) in shape and then linear. The increase in drain current, ID for a given increase in gate-source voltage, VGS determines the slope or gradient of the curve for constant values of VDS.
Then we can see that turning an enhancement MOS transistor "ON" is a gradual process and in order for us to use the MOSFET as an amplifier we must bias its gate terminal at some point above its threshold level.

There are many different ways we can do this from using two separate voltage supplies, to drain feedback biasing, to zener diode biasing, etc, etc. But whichever biasing method we use, we must make sure that the gate voltage is more positive than the source by an amount greater than VTH. In this MOSFET amplifier tutorial we will use the now familiar universal voltage divider biasing circuit.

**DC Biasing the MOSFET**

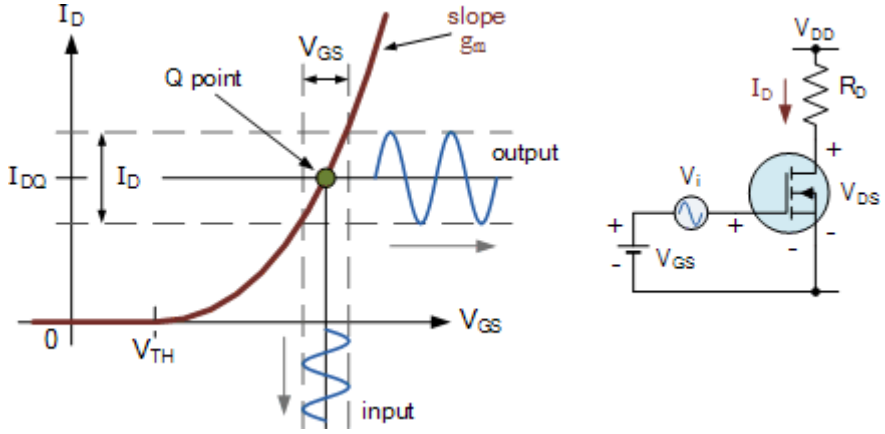
The universal voltage divider biasing circuit is a popular biasing technique used to establish a desired DC operating condition of bipolar transistor amplifiers as well as MOSFET amplifiers. The advantage of the voltage divider biasing network is that the MOSFET, or indeed a bipolar transistor, can be biased from a single DC supply. But first we need to know where to bias the gate for our MOSFET amplifier.
A MOSFET device has three different regions of operation. These regions are called the: Ohmic/Triode region, Saturation/Linear region and Pinch-off point. For a MOSFET to operate as a linear amplifier, we need to establish a well-defined quiescent operating point, or Q-point, so it must be biased to operate in its saturation region. The Q-point for the MOSFET is represented by the DC values, ID and VGS that position the operating point centrally on the MOSFETs output characteristics curve.

As we have seen above, the saturation region begins when VGS is above the VTH threshold level. Therefore if we apply a small AC signal which is superimposed on to this DC bias at the gate input, then the MOSFET will act as a linear amplifier as shown.
The common-source NMOS circuit above shows that the sinusoidal input voltage, Vi is in series with a DC source. This DC gate voltage will be set by the bias circuit. Then the total gate-source voltage will be the sum of VGS and Vi.The DC characteristics and therefore Q-point (quiescent point) are all functions of gate voltage VGS, supply voltage VDD and load resistance RD.

The MOS transistor is biased within the saturation region to establish the desired drain current which will define the transistors Q-point. As the instantaneous value of VGS increases, the bias point moves up the curve as shown allowing a larger drain current to flow as VDS decreases.

Likewise, as the instantaneous value of VGS decreases (during the negative half of the input sine wave), the bias point moves down the curve and a smaller VGS results in a smaller drain current and increased VDS.

**eMOSFET DC Bias Point**




Then in order to establish a large output swing we must bias the transistor well above threshold level to ensure that the transistor stays in saturation over the full sinusoidal input cycle. However, there is a limit on the amount of gate bias and drain current we can use. To allow for maximum voltage swing of the output, the Q-point should be positioned approximately halfway between the supply voltage VDD and the threshold voltage VTH.

So for example, lets assume we want to construct a single stage NMOS common-source amplifier. The threshold voltage, VTH of the eMOSFET is 2.5 volts and the supply voltage, VDD is +15 volts. Then the DC bias point will be 15 – 2.5 = 12.5v or 6 volts to the nearest integer value.

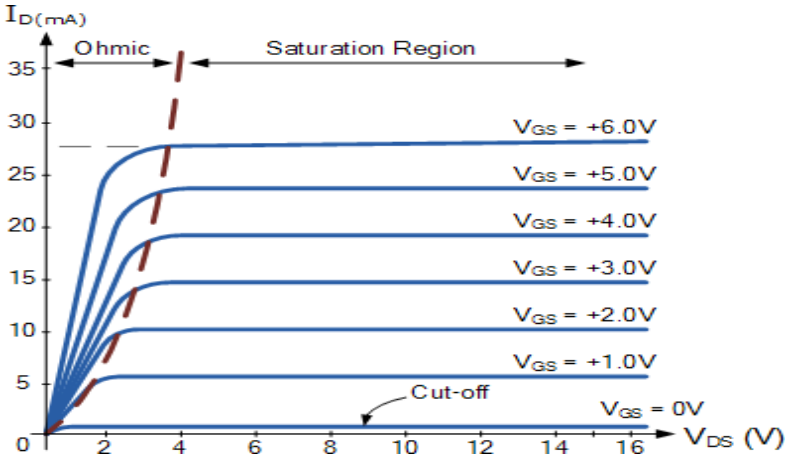
**MOSFETS ID – VDS Characteristics**

We have seen above that we can construct a graph of the MOSFETs forward DC characteristics by keeping the supply voltage, VDD constant and increasing the gate voltage, VG.

But in order to get a complete picture of the operation of the n-type enhancement MOS transistor to use within a MOSFET amplifier circuit, we need to display the output characteristics for different values of both VDD and VGS.

As with the NPN Bipolar Junction Transistor, we can construct a set of output characteristics curves showing the drain current, ID for increasing positive values of VG for an n-channel enhancement- mode MOS transistor as shown.

**N-type eMOSFET Characteristics**



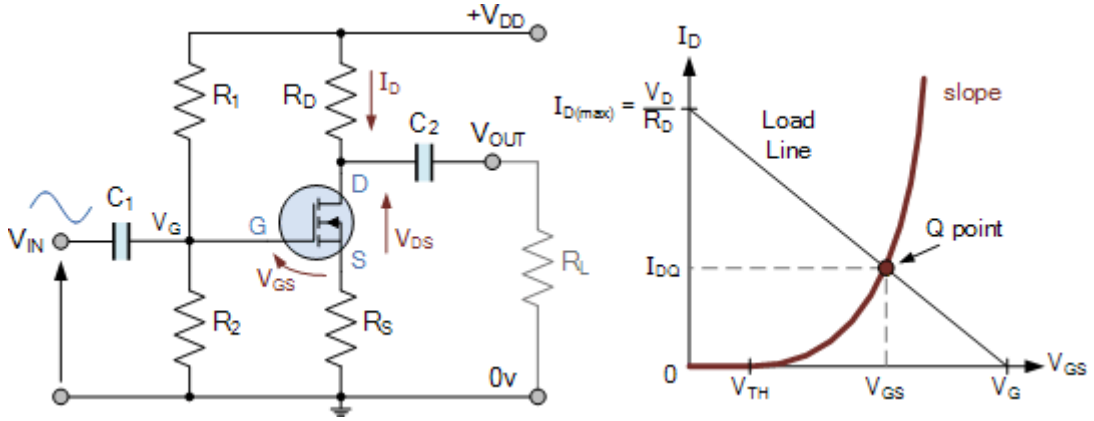
Note that a p-channel eMOSFET device would have a very similar set of drain current characteristics curves but the polarity of the gate voltage would be reversed.

**Basic Common Source MOSFET Amplifier**

Previously we look at how to establish the desired DC operating condition to bias the n-type eMOSFET. If we apply a small time-varying signal to the input, then under the right circumstances the MOSFET circuit can act as a linear amplifier providing the transistors Q-point is somewhere near the center of the saturation region, and the input signal is small enough for the output to remain linear. Consider the basic MOSFET amplifier circuit below.

**Basic MOSFET Amplifier**

This simple enhancement-mode common source MOSFET amplifier configuration uses a single supply at the drain and generates the required gate voltage, VG using a resistor divider. We remember that for a MOSFET, no current flows into the gate terminal and from this we can make the following basic assumptions about the MOSFET amplifiers DC operating conditions.




$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$
$$= I_D (R_D + R_S) + V_{DS}$$

$$\therefore R_D + R_S = \frac{V_{DD} - V_{DS}}{I_D}$$

Then from this we can say that:

$$R_D = \frac{V_{DD} - V_D}{I_D} \quad \text{and} \quad R_S = \frac{V_S}{I_D}$$
$$V_{GS} = V_G - I_S R_S$$

and the MOSFETs gate-to-source voltage, VGS is given as:

As we have seen above, for proper operation of the MOSFET, this gate-source voltage must be greater than the threshold voltage of the MOSFET, that is VGS > VTH. Since IS = ID, the gate voltage, VG is therefore equal too:

$$V_{GS} = V_G - I_D R_S$$

$$\therefore V_G = V_{GS} + I_D R_S$$

$$\text{or } V_G = V_{GS} + V_S$$

To set the MOSFET amplifier gate voltage to this value we select the values of the resistors, R1 and R2 within the voltage divider network to the correct values. As we know from above"no current" flows into the gate terminal of a MOSFET device so the formula for voltage division is given as:

$$V_G = V_{DD}\left(\frac{R_2}{R_1 + R_2}\right)$$

Note that this voltage divider equation only determines the ratio of the two bias resistors, R1 and R2 and not their actual values. Also it is desirable to make the values of these two resistors as large as possible to reduce their I2*R power loss and increase the MOSFET amplifiers input resistance.

**PROCEDURE:**

**1. Launch Multisim**

Open NI Multisim from your computer.

**2. Place Components on the Workspace**

Go to Place → Component and add the following:
NMOS transistor (e.g., 2N7000 or IRF540N), Resistors (R1, R2, RD, RS as per design), Capacitors (Coupling and bypass capacitors, e.g., C1, C2, CE), DC power supply (VDD) Function generator (AC input source), Ground, Oscilloscope or probe for observing signals

**3. Build the Common Source Amplifier Circuit**

- Connect the components as per this configuration:
- Input AC Signal → Through C1 to the Gate of the NMOS
- Drain Resistor (RD) connected between Drain and VDD
- Source Resistor (RS) connected between Source and Ground
- Bypass Capacitor (CE) parallel to RS (optional for gain)
- Gate Biasing Resistors (R1, R2) form a voltage divider between VDD and GND and connect to the Gate. Output taken from the Drain through C2.

**4. Set Component Values**

**5. Bias the MOSFET Properly**

Ensure VGS > Vth (threshold voltage) so that the MOSFET operates in the saturation region. Adjust R1 and R2 to provide a proper bias voltage at the Gate.

**6. Simulate the Circuit**

Click Run button (green play symbol). Use an oscilloscope to probe input and output signals.

7. **Observe the Output**

**Compare the input and output waveforms.**

Observe an amplified output signal at the drain (180° out of phase with input). Measure gain: Av = Vout / Vin

**8. Analyze**

Note the amplitude, phase shift, and gain.
Adjust component values and see their effect on the amplifier's performance.

**CIRCUIT DIAGRAM:**

**OBSERVATION TABLE**

| Sr.No. | Vin | Vo | Av=$\frac{Vo}{Vin}$ |
|---|---|---|---|
| | | | |

## CONCLUSION :

**Teacher Sign with Date** **Remark**

## POST LAB QUESTIONS:

1. What happens to the output signal if the bypass capacitor (CE) is removed?
2. What condition must be met for the MOSFET to operate in the saturation region? Why is this region preferred for amplification?
3. If the input signal frequency is increased, what happens to the gain and waveform?
4. What is the typical phase shift between input and output in a CS amplifier?
5. What is the role of the bypass capacitor in the CS amplifier circuit? How does it affect the gain?

## *Experiment No.7*

***Title:-***

***Division:-*** ***Batch:-*** ***Roll no:-***

***Date of performance:-*** ***Date of Submission:-***

# EXPERIMENT No.7

**Aim:** To study Astable multi-vibrator using IC 555 and calculate duty cycle and frequency of output.

**Apparatus:** Power supply , CRO

**Theory:**

IC 555 usually referred as timer IC, includes 23 transistors, 2 diodes and 16 resisters on in an 8-pin DIP. The three resistors each of 5KΩ, connected in series forming a voltage divider network gives it the name 555.

The LM555 generates accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. The IC could be externally triggered or reseted as per the need.

It can be used in many applications, example lamp flashers, pulse generation, ppm and multivibrator circuits.

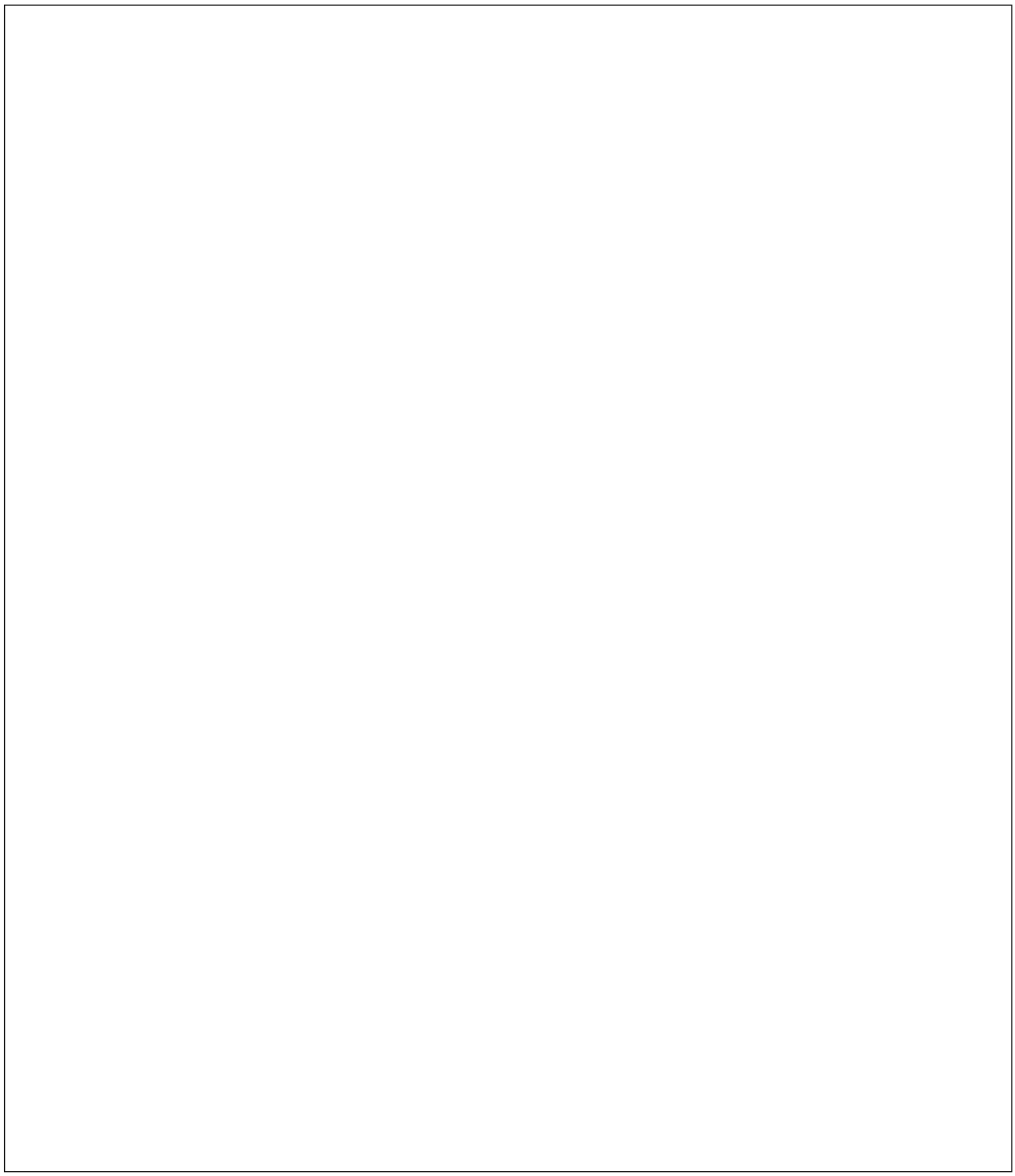
There are three multivibrator modes : Astable Mode, Monostable Mode and Bistable mode.

Astable Mode : The 555timer functions as an oscillator. Both states are quasi stable state. External trigger is not required. This mode is used for circuits such as LED and lamp flashers, pulse generators, logic clocks, tone generators and security alarms.

Monostable Mode : One stable state and other Quasi stable state. External trigger is required to change from stable state to quasi stable state. The timer 555 functions as a 'one-shot'. Applications include timers, missing pulse detectors, bounce free switches and touch switches.

Bistable Mode : Both the state are stable states, External trigger is required to change the state. No external component is required. Operate as flip flop

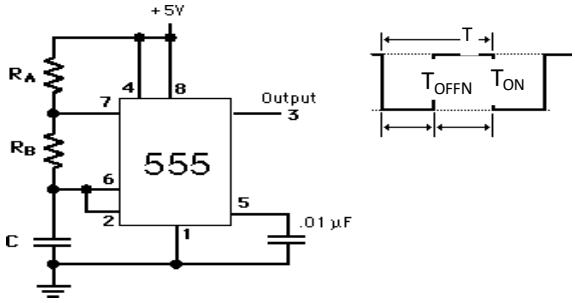
**CIRCUIT DIAGRAM:**



The voltage across internal resistive network holds the positive input of comparator two at 2/3Vcc and the positive input to comparator one at 1/3Vcc. The two comparators produce an output voltage dependent upon the voltage difference at their inputs which is determined by the charging and discharging action of the externally connected RC network. The outputs from both comparators are connected to the two inputs of the flip-flop which in turn produces either a "HIGH" or "LOW" level output at Q based on the states of its inputs. The output from the flip- flop is used to control a high current output switching stage to drive the connected load producing either a "HIGH" or "LOW" voltage level at the output pin.

**Astable multivibrator:**

The Astable multivibrator generates a square wave, the period of which is determined by the circuit external to IC 555. The astable multivibrator does not require any external trigger to change the state of the output, hence the name free running oscillator. The time during which the output is either high or low is determined by the two resistors and a capacitor which are externally connected to the 555 timer.




The figure shows the 555 timer connected as an astable multivibrator. Initially when the output is high capacitor C starts charging towards $V_{cc}$ through $R_A$ and $R_B$. However as soon as the voltage across the capacitor equals 2/3 $V_{cc}$ , comparator1 triggers the flip-flop and the output switches to low state. Now capacitor C discharges through $R_B$ and the internal transistor Q1. When voltage across C equals 1/3 $V_{cc}$, comparator 2's output triggers the flip- flop and the output goes high. Then the cycle repeats. The capacitor is periodically charged and discharged between 2/3 $V_{cc}$ and 1/3 $V_{cc}$ respectively.

The time during which the capacitor charges from 1/3 $V_{cc}$ to 2/3 $V_{cc}$ is equal to the time the output remains high and is given by

$$t_c = 0.69(R_A + R_B)C$$

Similarly the time during which the capacitor discharges from 2/3 Vcc to 1/3 Vcc is equal to the time the output is low and is given by

$$t_d = 0.69 R_B C$$

Thus the total time period of the output waveform is

$$T = t_c + t_d = 0.69(R_A + 2R_B)C$$

Therefore the frequency of oscillation

$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

The output frequency, $f$ is independent of the supply voltage $V_{cc}$.

**PROCEDURE:**

1. Find out the values of resistors and capacitors from board and calculate the theoretical frequency.
2. Make the connection as per circuit diagram.
3. Observe the voltage across the capacitor ($V_c$) and output ($V_o$) simultaneously on CRO.
4. Note down the time and voltage levels of $V_o$ and $V_c$.
5. Observe $T_{ON}$ and $T_{OFF}$ and calculate the duty cycle.
6. Draw the waveforms on Graph.

**OBSERVATION TABLE:**

$V_{cc}$ = $R_A$ = $R_B$ = $C_1$ =

| Type Of Multivibrator | O/P Frequency | Output Voltage | Minimum Voltage across capacitor | Maximum Voltage across capacitor |
|---|---|---|---|---|
| Astable Multivibrator | | | | |

| $T_{ON}$ | $T_{OFF}$ | T | Frequency |
|---|---|---|---|
| | | | |

**CALCULATION:**

$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

% Duty cycle=% D= $\frac{RA+RB}{RA+2RB}$ X100 = $\frac{Ton}{Ttotal}$ × 100 where Ttotal=Ton +Toff

**RESULT:**

| Type Of Multivibrator | Output frequency | | Duty Cycle | |
|---|---|---|---|---|
| | Theoretical | Practical | Theoretical | Practical |
| Astable Multivibrator | | | | |

**CONCLUSION:**

**Teacher Sign with Date** **Remark**

**REFERENCES:**

1. Op-Amps and Linear Integrated Circuits. Ramakant A. Gaikwad
2. Modern Digital Electronics. R. P. Jain

**POST LAB QUESTIONS**

1. What is a multivibrator circuit? What are its different types?
2. Mention various types of multivibrator.
3. Draw the internal diagram of IC 555. Show the pin numbers in the diagram.
4. What is an astable multivibrator?
5. What are the main applications of astable multivibrators?

## Experiment No.8

***Title:-***

***Division:-*** ***Batch:-*** ***Roll no:-***

***Date of Performance:-*** ***Date of Submission:-***

# EXPERIMENT No. 8

**Aim:** To study Inverting & Noninverting amplifier using OPAMP.

**Apparatus:** Bread Board, 741 IC, ±12V supply, Resistors and connecting leads.

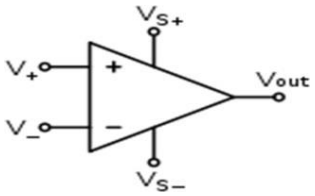
## Theory:

### OPERATIONAL AMPLIFIER

An operational amplifier, which is often called an op-amp, is a DC-coupled high-gain electronic voltage amplifier with differential inputs and, usually, a single output. Typically, the output of the op-amp is controlled either by negative feedback, which largely determines the magnitude of its output voltage gain, or by positive feedback, which facilitates regenerative gain and oscillation. High input impedance at the input terminals and low output impedance are important typical characteristics.

The op-amp is basically a differential amplifier having a large voltage gain, very high input impedance and low output impedance. The op-amp has an "Inverting" or (-) input and "Non-inverting" or (+) input and a single output. The op-amp is usually powered by a dual polarity power supply in the range of +/- 5 volts to +/- 15 volts. Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices.

**Circuit notation:**




The circuit symbol for an op-amp is shown in above Figure. where:

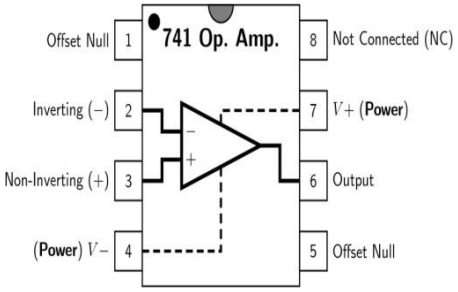
- $V_+$ : non-inverting input
- $V_S$ + : positive power supply
- $V_-$ : inverting input
- $V_S$ − : negative power supply
- $V_{out}$: output

The power supply pins ($V_S$ + and $V_S$ −) can be labeled in different ways. Despite different labeling, the function remains the same. Often these pins are left out of the diagram for clarity, and the power configuration is described or assumed from the circuit. For any input voltages the ideal op-amp has

- Infinite open-loop gain,
- Infinite slew rate,
- Infinite bandwidth,
- Zero output impedance,
- Infinite input impedances.
- zero noise.
- Zero offset voltage,

**CIRCUIT DIAGRAM:**

**Internal circuitry of 741 type op-amp**




Though designs vary between products and manufacturers, all op-amps have basically the same internal structure, which consists of three stages:

**Differential amplifier**

Input stage — provides low noise amplification, high input impedance, usually a differential output

Voltage amplifier

Provides high voltage gain, a single-pole frequency roll-off, usually single-ended output

Output amplifier

Output stage — provides high current driving capability, low output impedance, current limiting and short circuit protection circuitry

The 741 is usually supplied in an 8-pin 'DIL' (Dual In Line) or 'DIP' (Dual Inline Package, or sometimes Dual Inline Plastic) package with a pinout shown above. The values given below are 'typical' for an ordinary 741, better versions (more expensive) may give better results...

Typical values of Basic Parameters:

Rail voltages: +/- 15V dc (+/- 5V min, +/- 18V max) Input impedance: Around 2MΩ

Low Frequency voltage gain: approx 200,000 Input bias current: 80nA

Slew rate: 0.5V per microsecond Maximum output current: 20mA

Recommended output load: not less than 2KΩ

**INVERTING AMPLIFIER USING 741:**

An inverting amplifier using op-amp is a type of amplifier using op-amp where the output waveform will be phase opposite to the input waveform. The input waveform will be amplifier by the factor Av (voltage gain of the amplifier) in magnitude and its phase will be inverted. In the inverting amplifier circuit the signal to be amplified is applied to the inverting input of the op-amp through the input resistance R1.

Rf is the feedback resistor. Rf and Rin together determine the gain of the amplifier. Inverting operational amplifier gain can be expressed using the equation Av = – Rf/R1. Negative sign implies that the output signal is negated. The circuit diagram of a basic inverting amplifier using op-amp is shown below.

**OBSERVATION TABLE:**

**A) Inverting Amplifier**

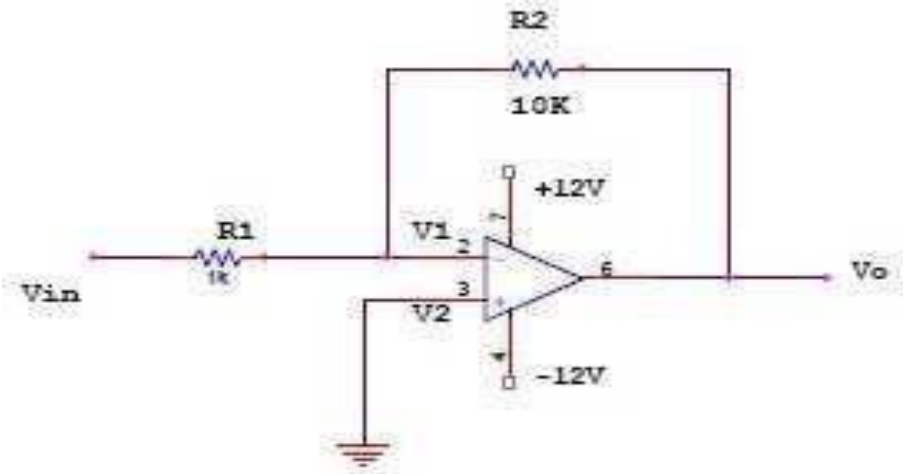
$R_1$= 1KΩ, $R_F$= 10KΩ, $V_{CC}$=+12V, $V_{EE}$=-12V

| Sr.No. | Input Voltage Vin (Vdc) | Output Voltage (Vo) | Voltage Gain Av = $-\frac{Vo}{Vin}$ |
|---|---|---|---|
| 1 | 0.1 | | |
| 2 | 0.2 | | |
| 3 | 0.3 | | |
| 4 | 0.4 | | |
| 5 | 0.5 | | |
| 6 | 0.6 | | |
| 7 | 0.7 | | |
| 8 | 0.8 | | |
| 9 | 0.9 | | |
| 10 | 1.0 | | |

**B) Non Inverting Amplifier**

$R_1$= 1KΩ, $R_F$= 10KΩ, $V_{CC}$=+12V, $V_{EE}$=-12V

| Sr.No. | Input Voltage Vin (Vdc) | Output Voltage (Vo) | Voltage Gain Av = $-\frac{Vo}{Vin}$ |
|---|---|---|---|
| 1 | 0.1 | | |
| 2 | 0.2 | | |
| 3 | 0.3 | | |
| 4 | 0.4 | | |
| 5 | 0.5 | | |
| 6 | 0.6 | | |
| 7 | 0.7 | | |
| 8 | 0.8 | | |
| 9 | 0.9 | | |
| 10 | 1.0 | | |




INVERTING AMPLIFIER

IC uA 741 has high performance and is the most popular operational amplifier.Signal to be amplified is applied to the inverting pi (pin2) of the IC. Non inverting pin (pin3) is connected to ground. R1 is the input resistor and Rf is the feedback resistor. Rf and R1 together sets the gain of the amplifier. With the used values of R1 and Rf the gain will be 10 (10K/1K = 10).

In the inverting amplifier only one input is applied to the inverting input (V2) terminal. The Non inverting input terminal (V1) is grounded.

Since, V1=0 V& V2=Vin , Vo= -Av X Vin

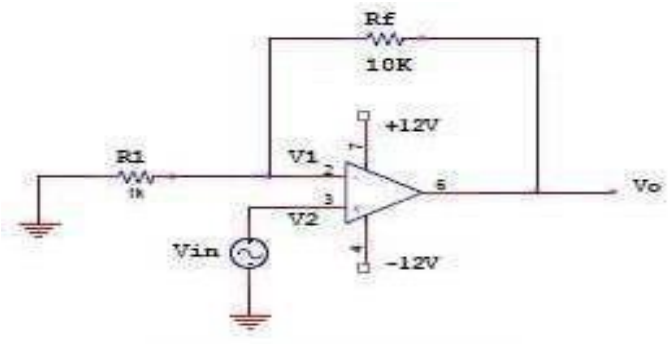
The negative sign indicates the output voltage is 1800 out of phase with respect to the input and amplified by gain Av.

**NON-INVERTING AMPLIFIER USING 741:**

The input is applied to the non-inverting input terminal and the Inverting terminal is connected to the ground.

V1= Vin & V2=0 Volts Vo= Av Vin

The output voltage is larger than the input voltage by gain Av & is in phase with the input signal.




NON-INVERTING AMPLIFIER

**CALCULATION:**

| **INVERTING AMPLIFIER** | **NON-INVERTING AMPLIFIER** |
|---|---|
| **Voltage Gain Av** $= -\frac{Rf}{R1}$ | **Voltage Gain Av** $= 1 + \frac{Rf}{R1}$ |

## CONCLUSION:

**Teacher Sign with Date** **Remark**

## REFERENCES:

1. Op-Amps and Linear Integrated Circuits. Ramakant A. Gaikwad
2. Modern Digital Electronics. R. P. Jain

## POST LAB QUESTIONS

1. Explain the Virtual ground concept of OP-AMP.
2. Draw and explain the block diagram of OP-AMP.
3. Explain different parameter of OP-AMP. State the different application of OP-AMP.
4. What is meant by negative feedback? What are the advantages and disadvantages of negative feedback?
5. State different application of OP-AMP.